

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicants: Hansen et al. )  
Serial No: 09/922,319 )  
5 Filing Date: August 2, 2001 ) Examiner: Unassigned  
Title: System with Wide Operand ) Group Art Unit: 2671  
Architecture, and Method )

Assistant Commissioner for Patents

10 Washington, D.C. 20231

**LETTER TO THE OFFICIAL DRAFTSMAN**

Dear Sir:

15 In response to the Notice to File Corrected Application Papers mailed August  
20, 2001, Applicants respectfully submit the following letter:

**Substitute Drawings**

20 By the Notice to File Corrected Application Papers mailed August 20, 2001, the  
Initial Patent Examination Division noted that "[s]ubstitute drawings in compliance  
with 37 CFR 1.84 [need to be submitted] because . . . drawing sheets do not have the  
appropriate margin(s) (see 37 CFR 1.84(g))."

25 Please substitute Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11 as filed on August 2,  
2001, with the enclosed substitute drawing sheets Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 10,  
and 11. Thus, Applicants respectfully submit that the substitute drawing sheets for  
Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11 comply with 37 CFR 1.84. Applicants  
respectfully submit that no new matter has been added by the replacement of the sheets  
of drawings.

30 **Conclusion**

It is therefore clear that Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11 comply with  
37 C.F.R. 1.84. The Commissioner is authorized to charge deposit account 50-0385 for  
any expenses, including extension fees, and/or to credit any overpayment to this  
account in connection with the transmittal of the drawings.

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In the event that any issue remains unresolved, the Official Draftsman is invited to telephone the undersigned at 650-233-5559.

Respectfully Submitted,



Leonard T. Guzman

Reg. No. 46,308

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Date: October 19, 2001

McDermott, Will & Emery


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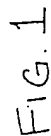
Phone: 650-233-5559

Facsimile: 650-233-5599

FOOTNOTES



# Block diagram



Chip boundary

# Wide multiply matrix

$$\blacksquare \text{rd}_{128} = \text{m}[\text{rc}]_{(128 \times 64/\text{size})} * \text{rb}_{128}$$

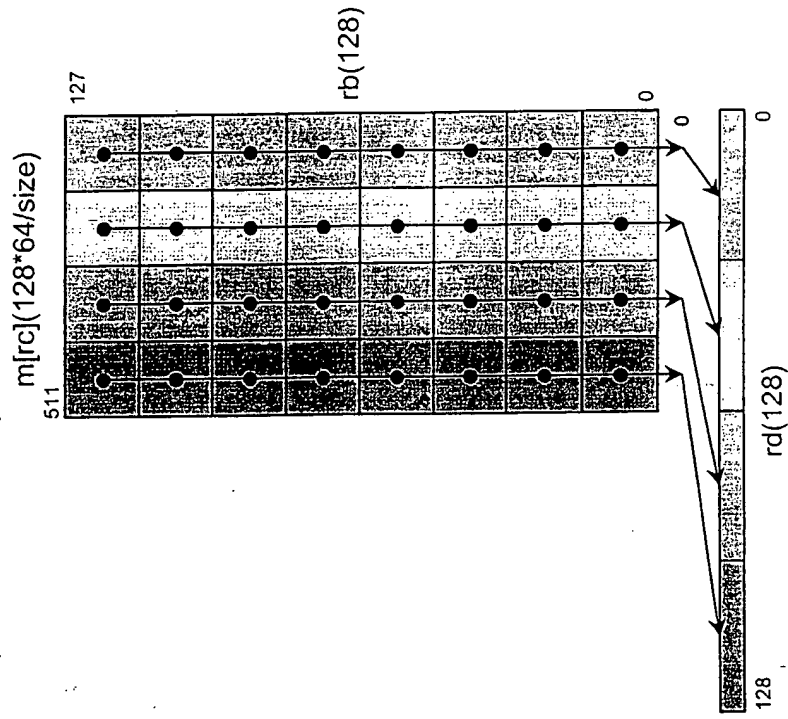


FIG. 2

# Wide multiply matrix

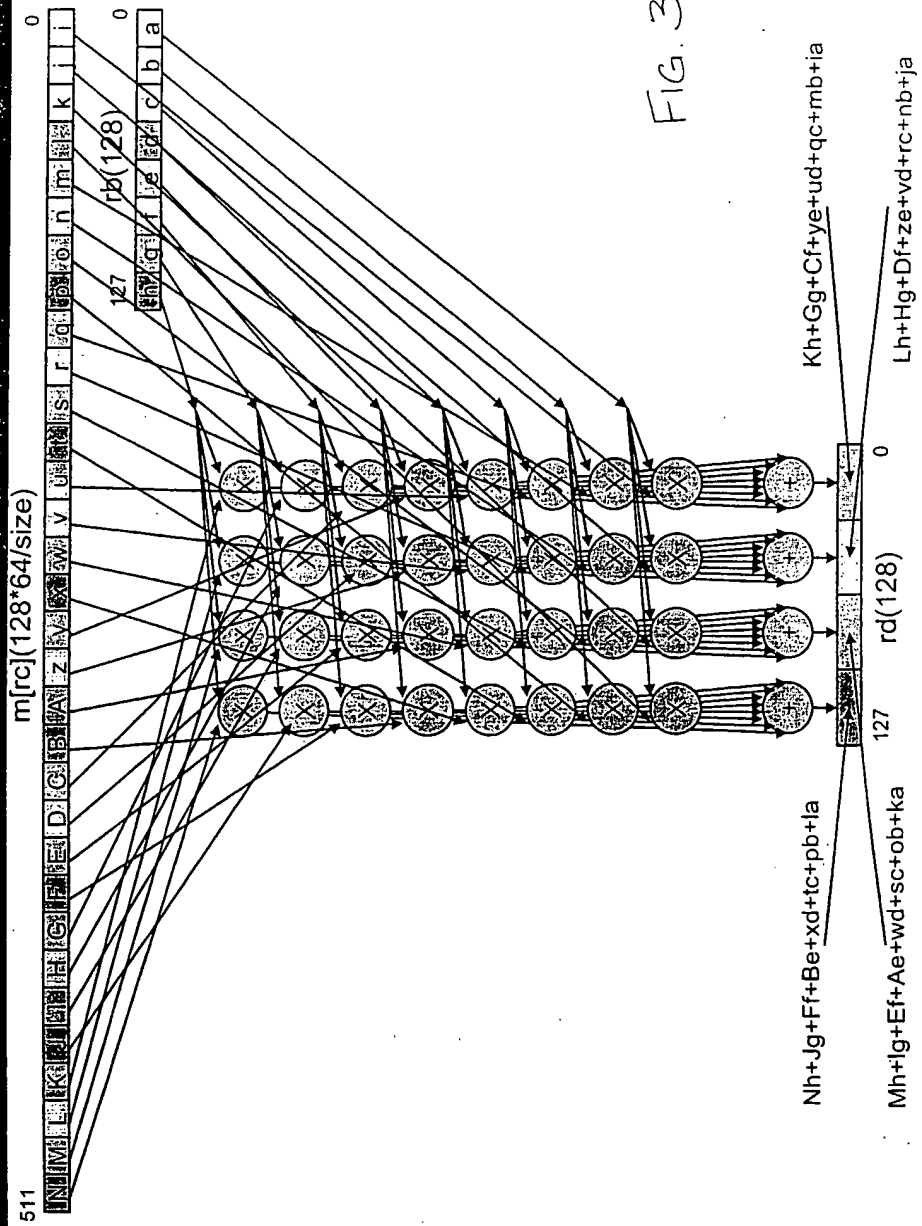
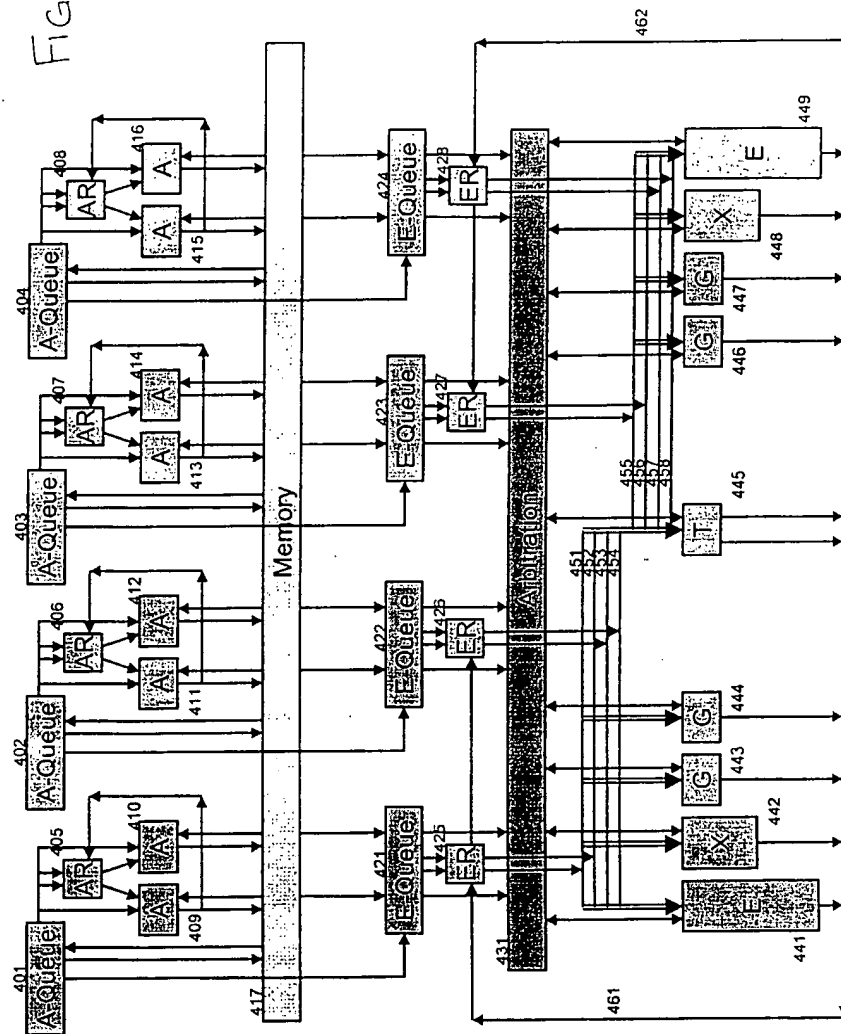


FIG. 3

# SMT + DAE

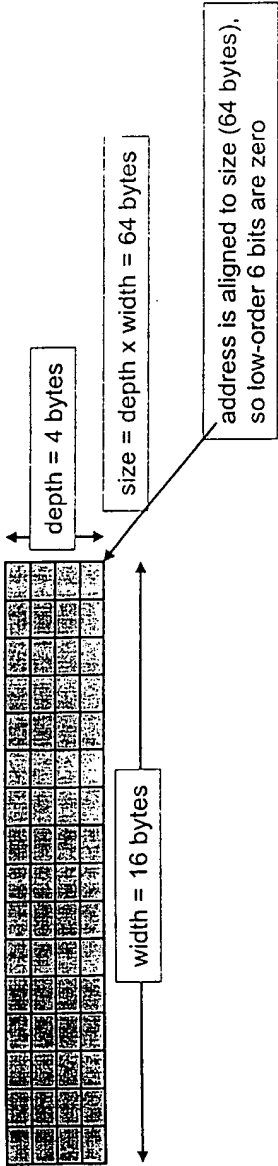
FIG. 4



# Wide operand specifier

■ specifier=address+(size/2)+(width/2)

FIG. 5



address

aaaaaaaaaaaaaaaaaaaaaaaaaaaa00000000

size/2

00000000000000000000000000000000

width/2

00000000000000000000000000000000

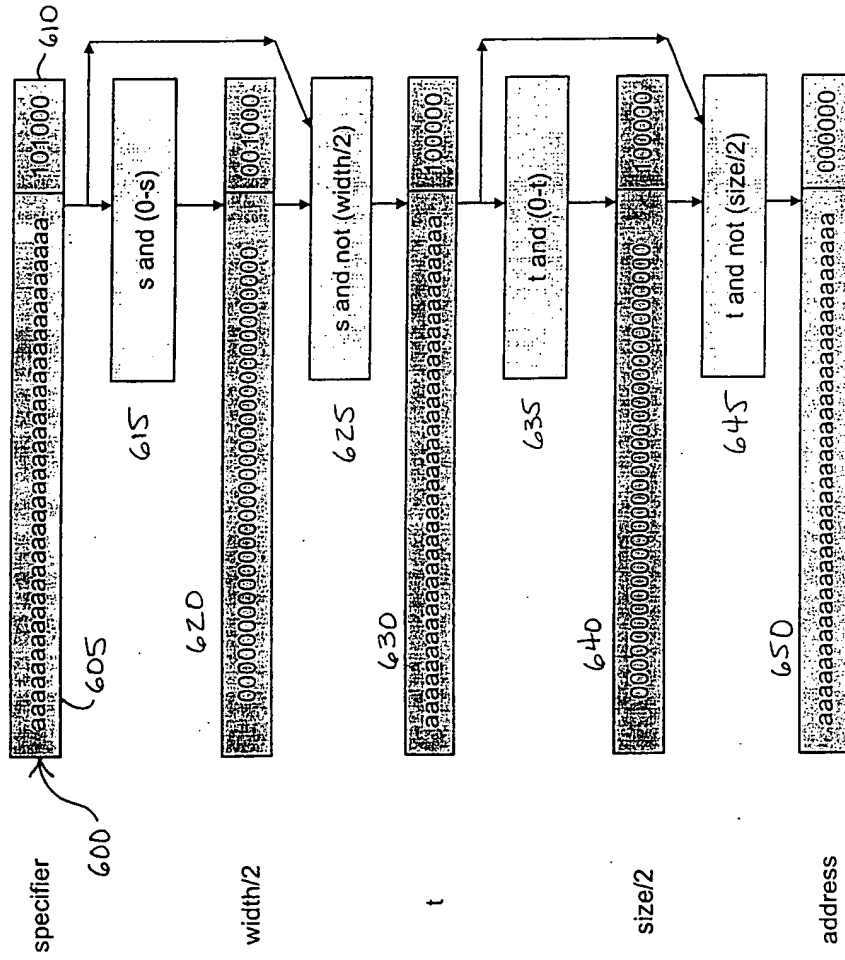
specifier

500 →

aaaaaaaaaaaaaaaaaaaaaaaaaaaa101000

510

# Specifier decoding

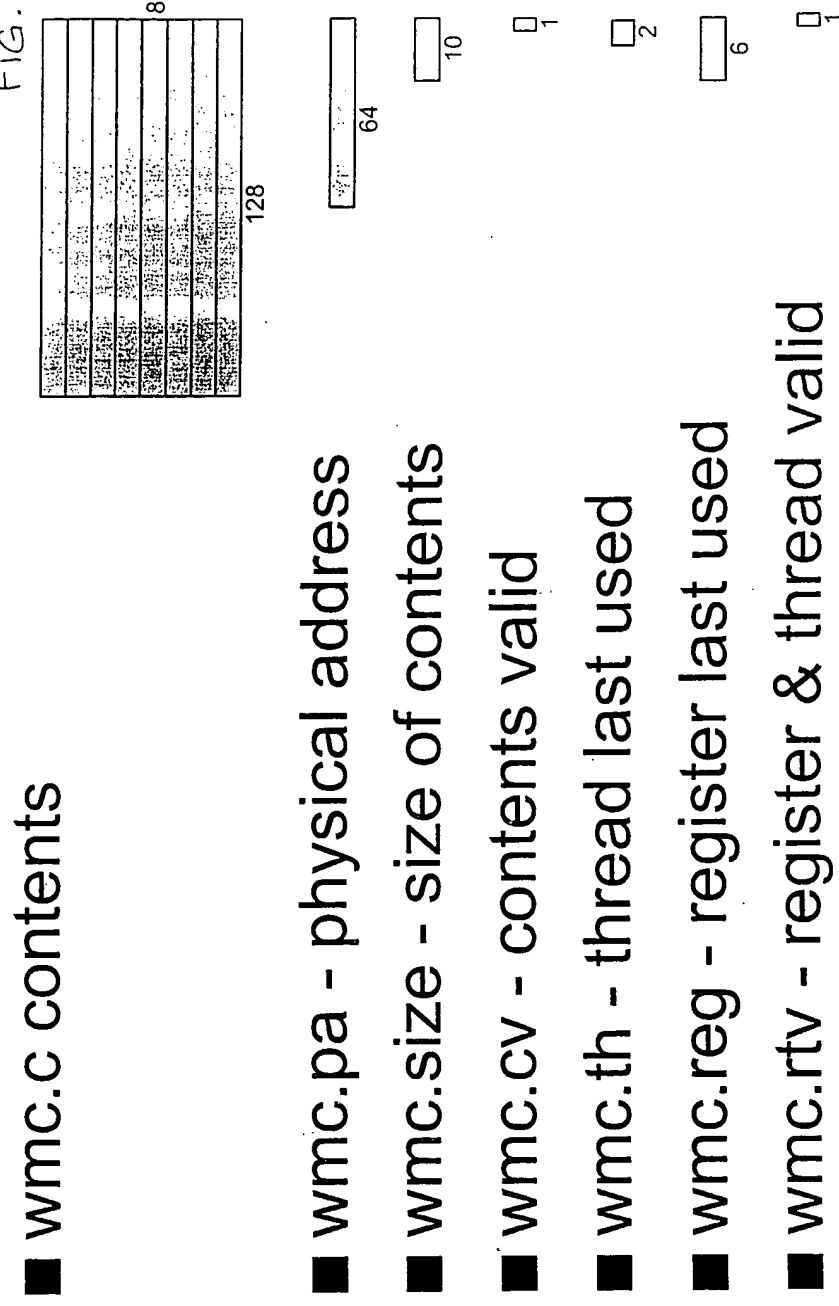






## Wide MicroCache data structures

FIG. 9





## Wide MicroCache control (2)

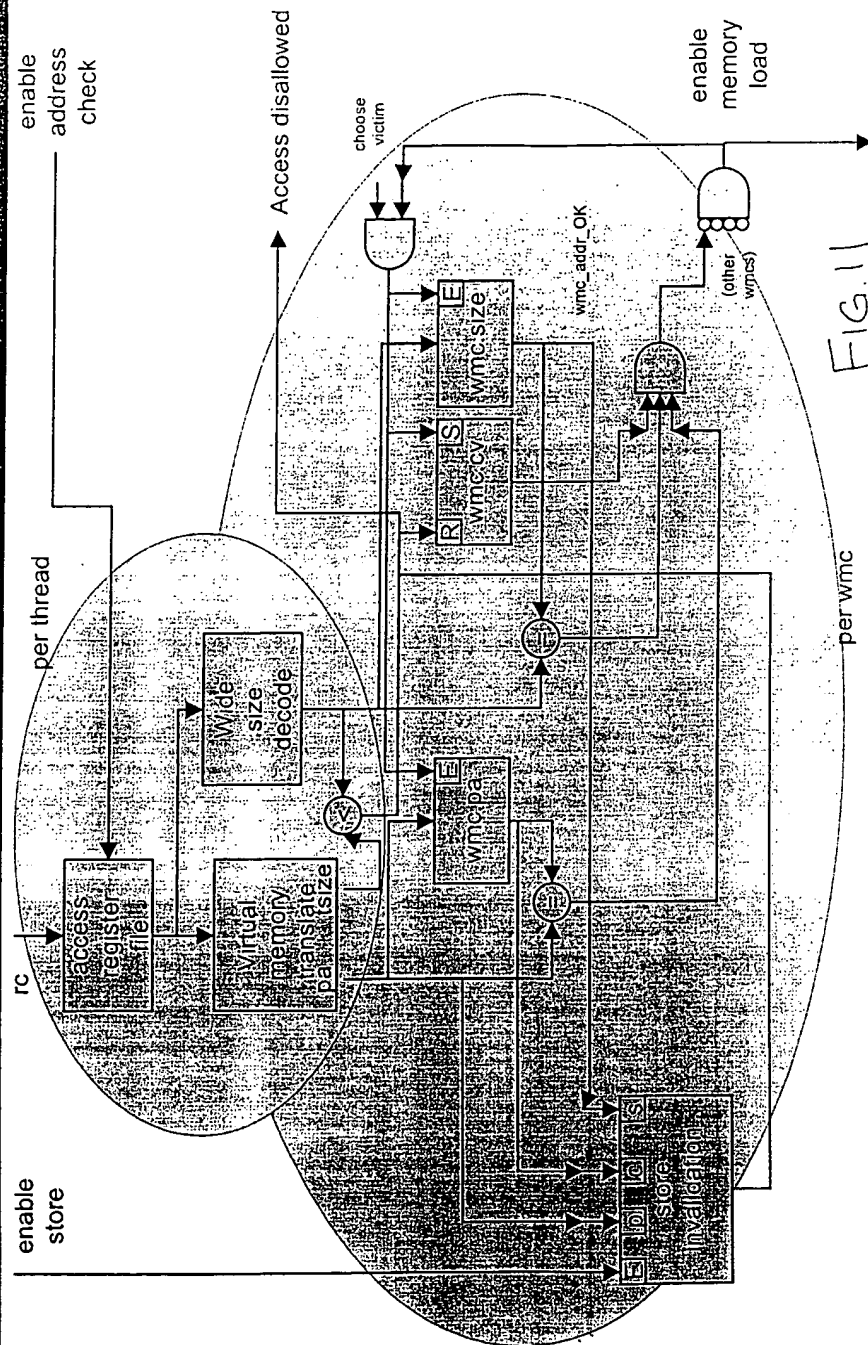


Fig. 11